BRCM24C32SC SOP-8 32 Kbit I²C

The BRCM24C32SC is 32Kbit I^{2}C-compatible Serial EEPROM (Electrically Erasable Programmable Read-Only Memory) device in a SOP-8 Plastic Package. Halogen-free Product.

1.7V 2.5~5.5V 1Mhz 1.7~2.5V
400Khz
CMOS 400uA 1.6mA

. Ì

Pin	Name	Type	Description
1	E0	Input	
2	E1	Input	
3	E2	Input	
4	GND	Ground	
5	SDA	I/O	/
6	SCL	Input	
7	WCB	Input	
8	VCC	Power	

/ See Marking Instructions

Parameter	Symbol	Rating	Unit
Storage Temperature	T_{stg}	-65~+150	
Operation Temperature	T_{opr}	-40~+85	
Maximum Operation Voltage	V_{cc}	6.25	V
Voltage on Any Pin with Respect to Ground	V_{pin}	-1.0~ Vcc+1.0	V
DC Output Current	I_{out}	5.0	mA
Electro-Static discharge HBM mode	ESD	6000	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Endurance	EDR	25 3.3V Page mode	1,000,000			Write cycles
Data retention	DRET		100			Years

Parameter	Symbol	1.7V≤Vcc<2.5V			2.5V≤Vcc≤5.5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Data In Hold Time	$t_{HD.DAT}$	0	-	-	0	-	-	us
Data In Setup Time	$t_{SU.DAT}$	0.1	-	-	0.1	-	-	us
Inputs Rise Time[1]	t_R	-	-	0.3	-	-	0.3	us
Inputs Fall Time[1]	t_F	-	-	0.3	-	-	0.1	us
Stop Setup Time	$t_{SU.STO}$	0.6	-	-	0.25	-	-	us
Data Out Hold Time	t_{DH}	0.05	-	-	0.05	-	-	us
WCB pin Setup Time	$t_{SU.WCB}$	1.2	-	-	0.6	-	-	us
WCB pin Hold Time	$t_{HD.WCB}$	1.2	-	-	0.6	-	-	us
Write Cycle Time	t_{WR}	-	-	5	-	-	5	ms

Notes:AC measurement conditions:

1. RL (connects to Vcc): 1.3k (2.5V, 5.5V), 10k (1.7V)
2. Input pulse voltages: 0.3 Vcc to 0.7 Vcc
3. Input rise and fall times: ≤50ns
4. Input and output timing reference voltages: 0.5Vcc

SDA SDA SCL (1) SCL
SDA (1)

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

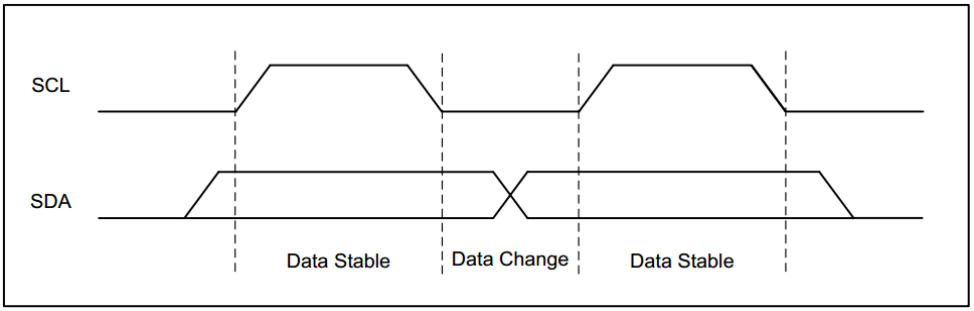


Figure 1 Data Validity

SCL SDA
2

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2).

SCL SDA
BRCM24C32SC

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the BRCM24C32SC in a standby power mode (see Figure 2).

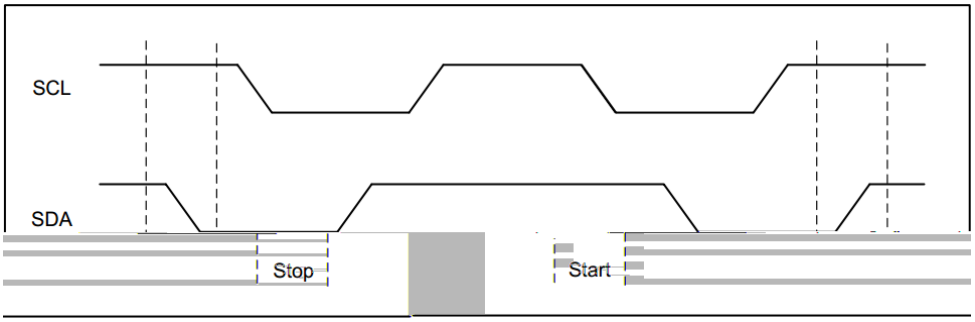
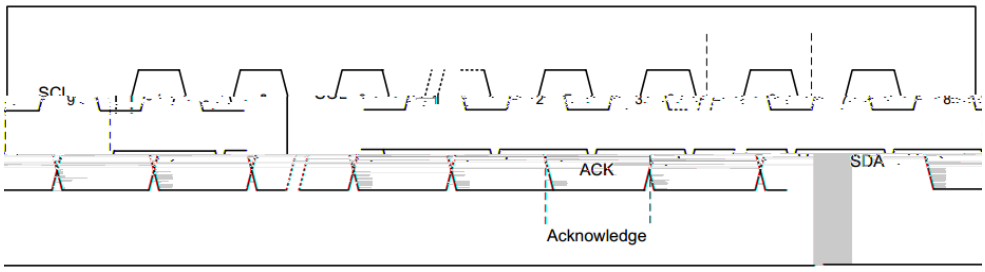


Figure 2 Start and Stop Definition

BRCM24C32SC BRCM24C32SC “ 0 ”
ACK 9

All addresses and data words are serially transmitted to and from the BRCM24C32SC in 8-bit words. The BRCM24C32SC sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.



Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCM24C32SC	Normal Area	1	0	1	0	E2	E1	E0	R/W
	ID Page	1	0	1	1	E2	E1	E0	R/W
	Lock Bit	1	0	1	1	E2	E1	E0	R/W
	Serial Number	1	0	1	1	E2	E1	E0	1

Table 1 Device Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCM24C32SC	Normal Area	X	X	X	X	A11	A10	A9	A8
	ID Page	X	X	X	X	0	0	X	X
	Lock Bit	X	X	X	X	X	1	X	X
	Serial Number	X	X	X	X	1	0	X	X

Table 2 First Word Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCM24C32SC	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	X	X	X	A4	A3	A2	A1	A0
	Lock Bit	X	X	X	X	X	X	X	X
	Serial Number	X	X	X	X	A3	A2	A1	A0

Table 3 Second Word Address

E2 E1 E0 8 E2 E1
E0 8 /
0 1 0

The E2, E1 and E0 device address bits to allow as many as 8 devices on the same bus. These bits must compare to their corresponding hardwired input pins. The E2, E1 and E0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

BRCM24C32SC WCB Vcc
BRCM24C32SC has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

8
BRCM24C32SC “ 0 ” 8 8
BRCM24C32SC “ 0 ”
BRCM24C32SC BRCM24C32SC
(5)

The lower five bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the BRCM24C32SC, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

BRCM24C32SC

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:
(a)Device type identifier = 1011b.
(b)Address bit A10 must be '1' all other address bits are don't care.
(c)The data byte must be equal to the binary value xxxx xx1x, where x is don't care.

/ / " 1 "
;

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: Current Address Read; Random Address Read and Sequential Read.

1

/ " 1 " BRCM24C32SC
" 0 " 7

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the BRCM24C32SC, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure7).

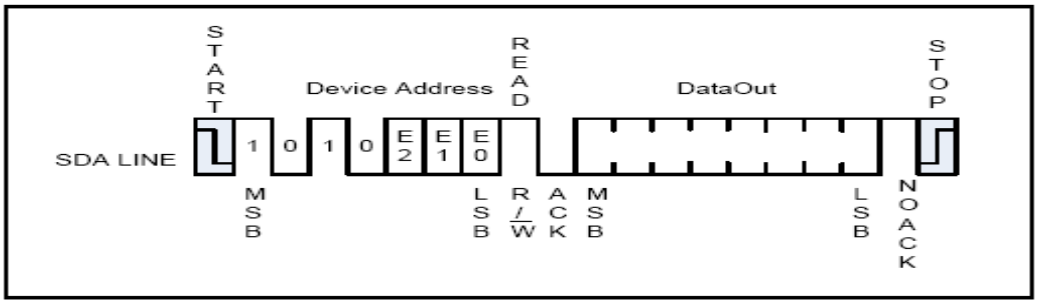


Figure 7 Current Address Read

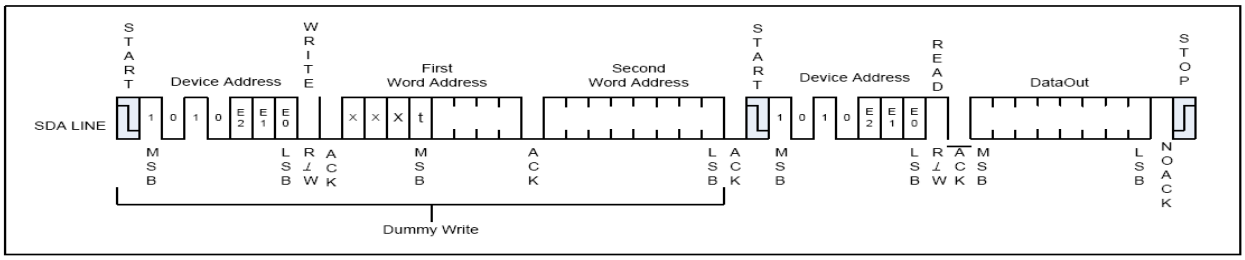
" "

BRCM24C32SC /

BRCM24C32SC

" 0 " 8

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the BRCM24C32SC,the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The BRCM24C32SC acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 8).



Notes: [1] x means don’t care bits.

[2] t means don’t care bit for BRCM24C32SC

Figure 8 Random Address Read

BRCM24C32SC

“ 0 ”

9

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the BRCM24C32SC receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 9).

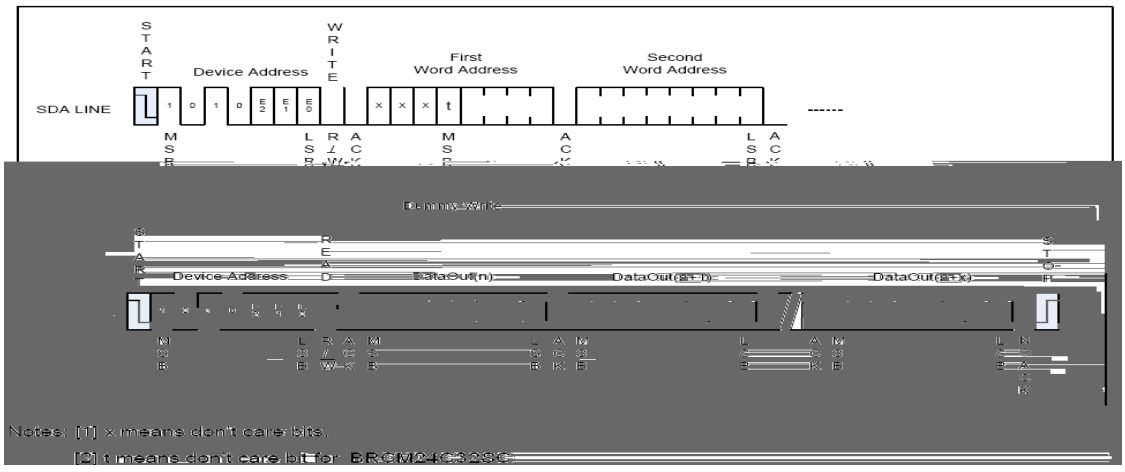


Figure 9 Sequential Read

32

1011b A15 / A5 A4 / A0 ID
10d 22 ID
32

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A15/A5 are don't care, the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

[+] /
ACK NoACK,(10)

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked (see Figure 10).

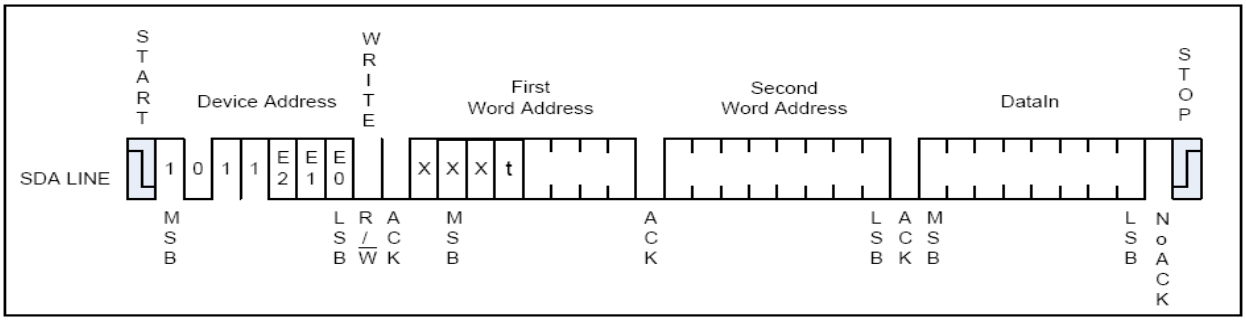


Figure 10 Lock Status Read (When Identification page locked, return NoACK after one data byte)

1
128
EEPROM " "
EEPROM
1

A11 A10 “ 10 ” 2 “ 10 ”

0800h

128 16

128 ACK

11

Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 1 , a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a ‘ 10 ’ sequence in bit A11 and A10 of the word address, regardless of the intended address as depicted in Table 2 . If a word address other than ‘ 10‘ is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will result in repeated serial number data readout for the data word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 11)

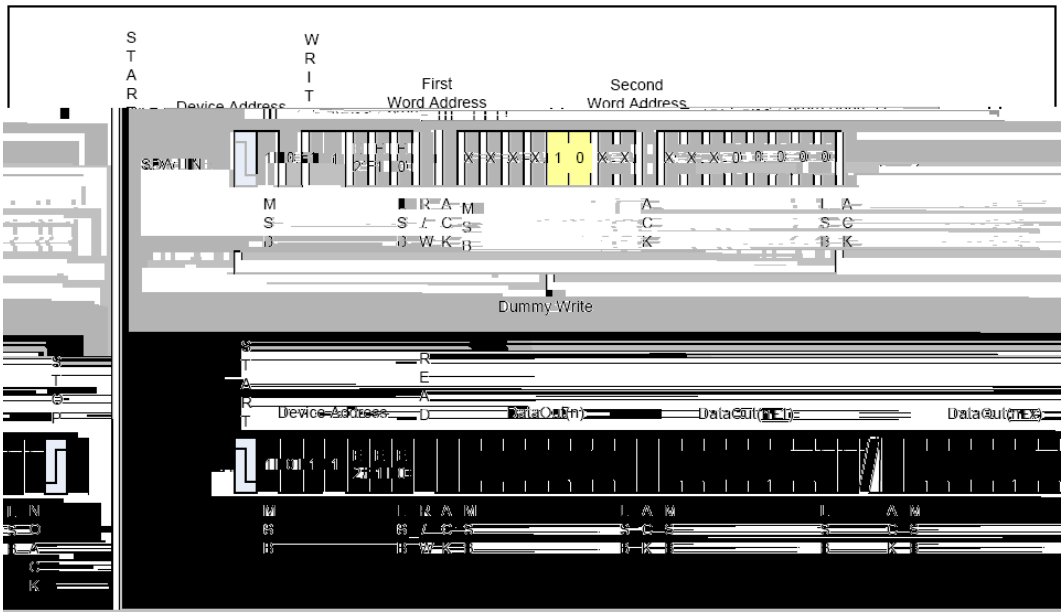
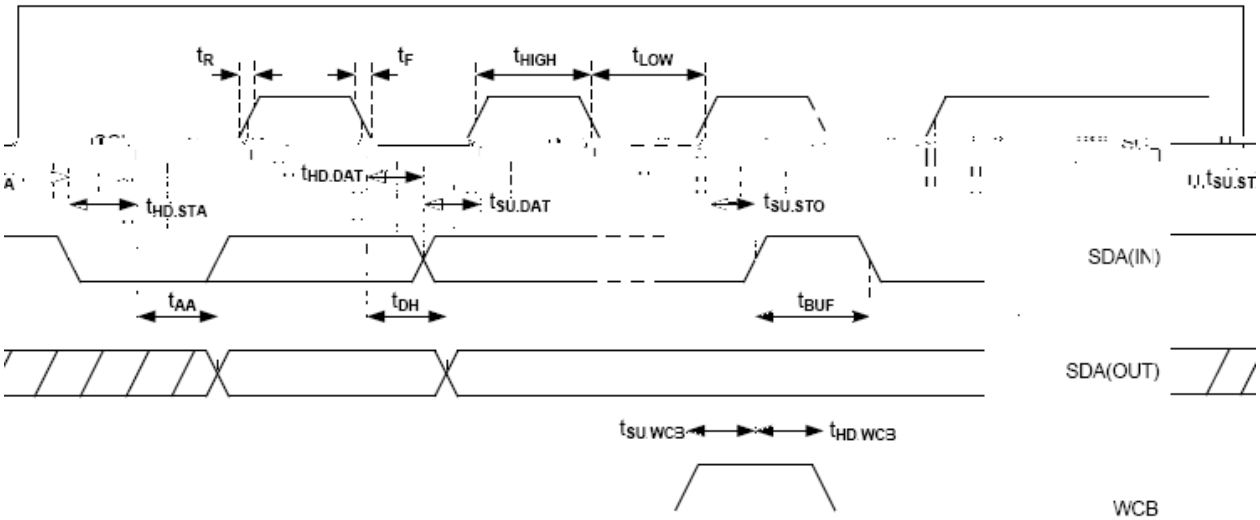
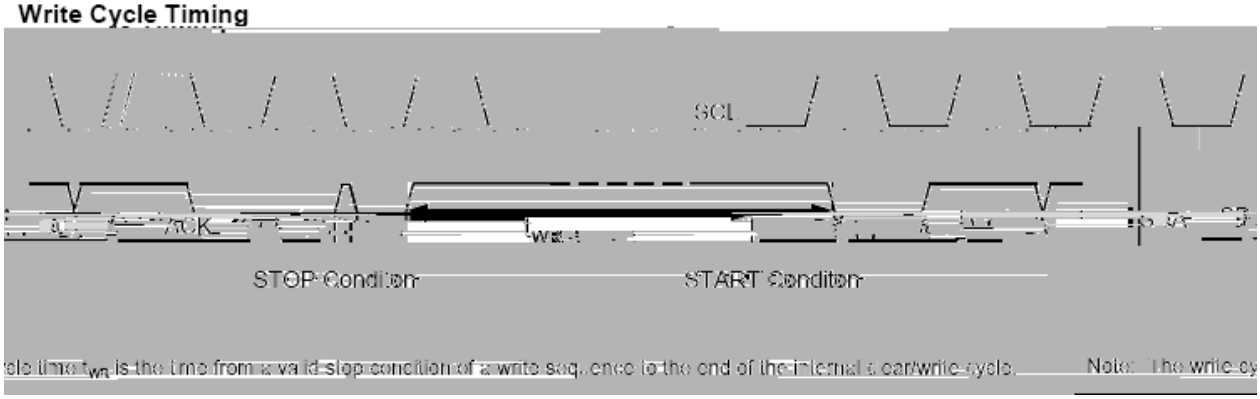


Figure 11 Sequential Read

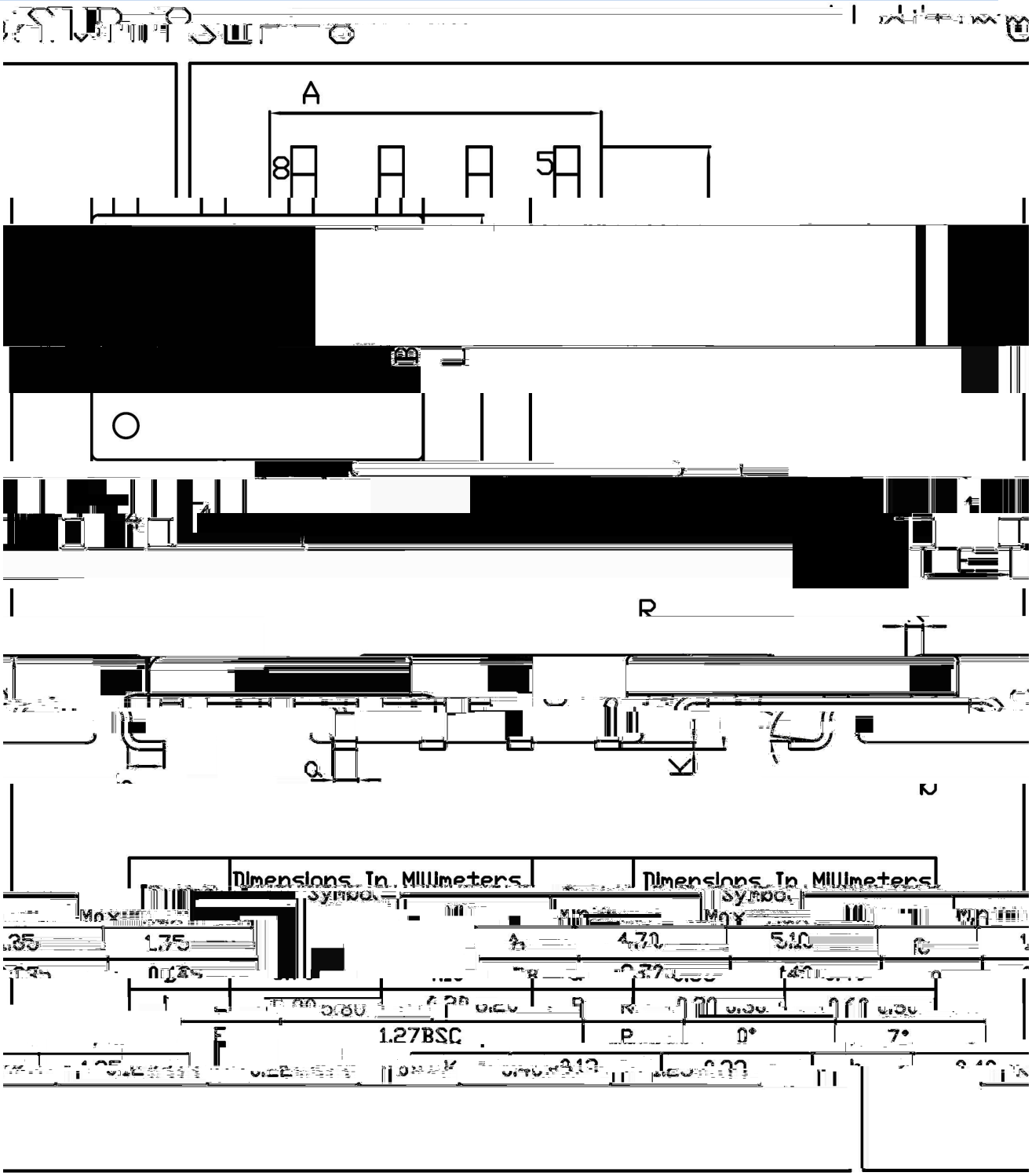
Bus Timing

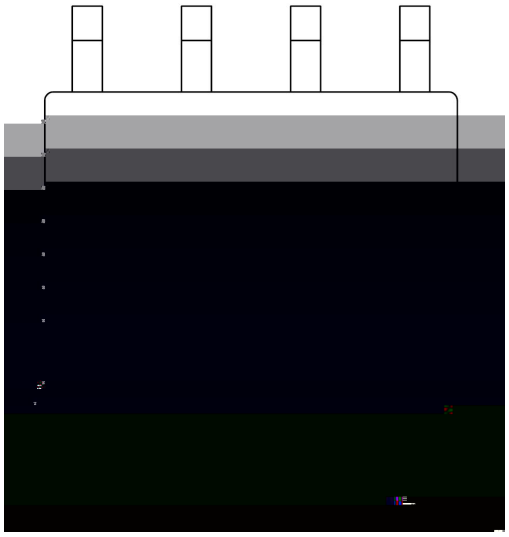


Write Cycle Timing



cle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/write cycle. Note: The write cy


A
Dimensions In Millimeters
Dimensions In Millimeters
1.75
4.70
5.10
1.27BSC
0°
7°



BR

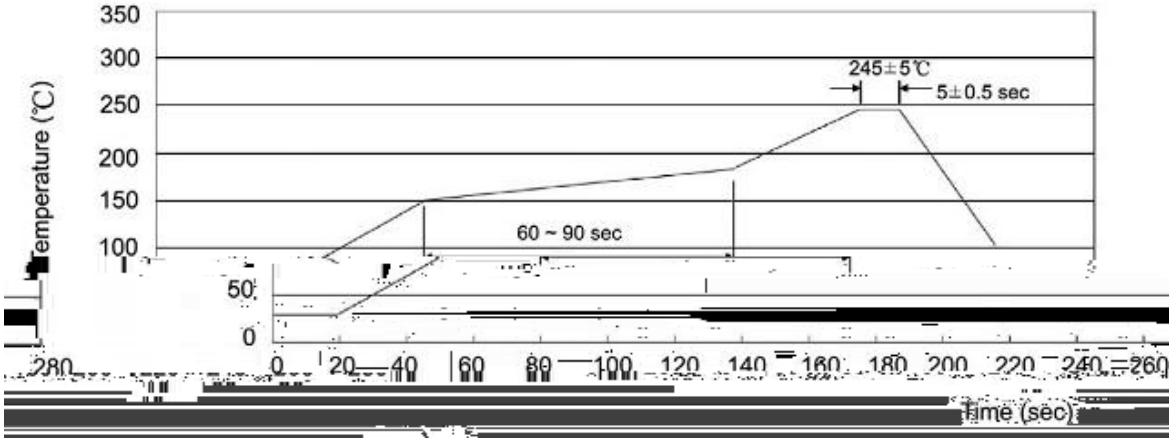
24C32

****

Note:

BR: Company Code.

24C32: Product Type.



		Note:	
1	150 180 60 90sec;	1.Preheating:150~180 , Time:60~90sec.	
2	245±5 5±0.5sec;	2.Peak Temp.:245±5 , Duration:5±0.5sec.	
3	2 10 /sec.	3. Cooling Speed: 2~10 /sec.	

260±5 10±1 sec. Temp.:260±5 Time:10±1 sec

/ REEL

Package Type 封装形式	Units 包装数量					Dimension 包装尺寸 (unit: mm^3)		
	Units/Reel 只/卷盘	Reels/Inner Box 卷盘/盒	Units/Inner Box 只/盒	Inner Boxes/Outer Box 盒/箱	Units/Outer Box 只/箱	Reel	Inner Box 盒	Outer Box 箱
SOP/ESOP-8	4,000	2	8,000	6	48,000	13 ×12	360×360×50	380×335×366