

BRCM24C04SC

SOP-8

4 Kbit

I²C

1.7V

2.5~5.5V

1Mhz

1.7~2.5V

400Khz

CMOS

400uA

1.6mA

16

128

5ms

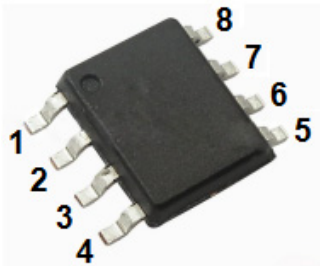
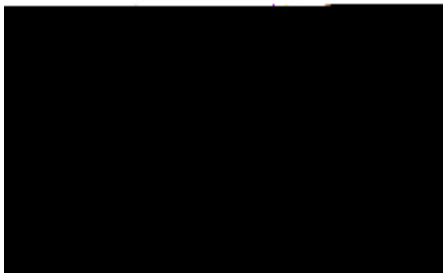
100

100

ESD HBM

6KV

+/-200mA;



Pin	Name	Type	Description
1	NC	-	
2	E1	Input	
3	E2	Input	
4	GND	Ground	
5	SDA	I/O	/
6	SCL	Input	
7	WCB	Input	
8	VCC	Power	

			mA
			V

		Ñ				

[illegible][illegible]

[illegible]

(1) SCL

Figure 1 Data Validity

SDA

SDA

BRCM24C04SC

Figure 2 Start and Stop Definition

“ 0 ”

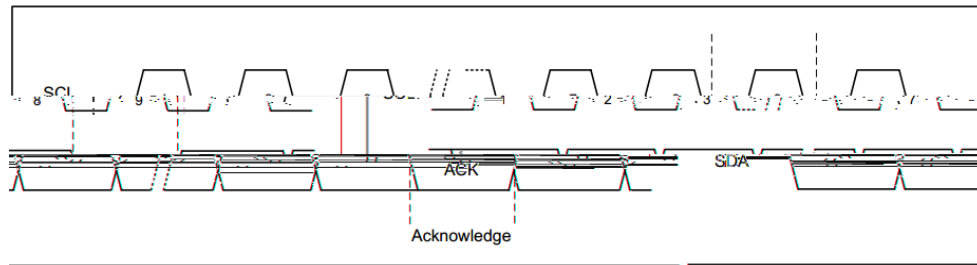


Figure 3 Output Acknowledge

H

BRCM24C04SC

:(a)

,(b)

E2E1

0

4

1

8

/

E2E1

0

H

BRCM24C04SCWCBVcc

H

8

BRCM24C04SC

“ 0 ”

8

8

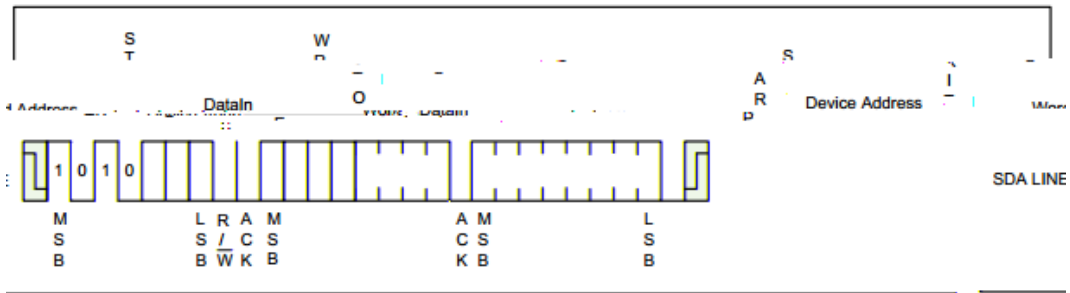
BRCM24C04SC

“ 0 ”

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(5)

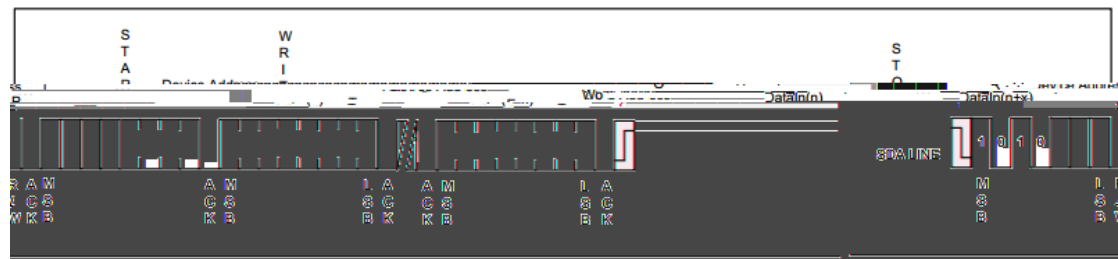


H

BRCM24C04SC

" 0 "

BRCM24C04SC



4

BRCM24C04SC

16

H

BRCM24C04SC

“ 0 ”

/

BRCM24C04SC

H

16

(a)

1011b

(b)

A5 / A4

0 1

A7 / A6

“ 00 ”

(c)

A3 / A0

NoACK

H

ID

Lock ID

(a)

1011b;

(b)

A6

1

;

(c)

xxxx xx1x

x

0

1

H
/
;
/ “ 1 ”

H
1
/ “ 1 ”
“ 0 ”
BRCM24C04SC
7

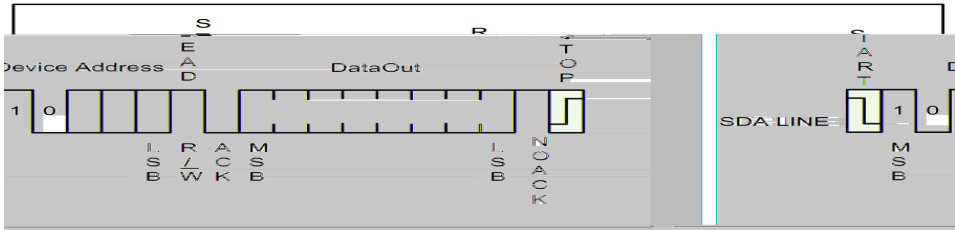
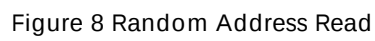


Figure 7

H
“ ”
BRCM24C04SC
/

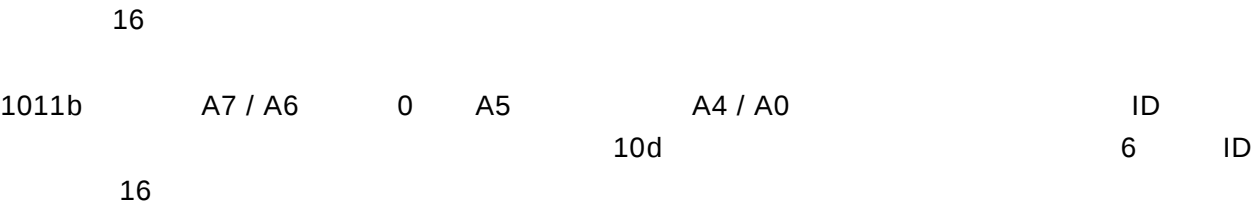
BRCM24C04SC
“ 0 ”
8



“ 0 ”

Figure 9

H



H

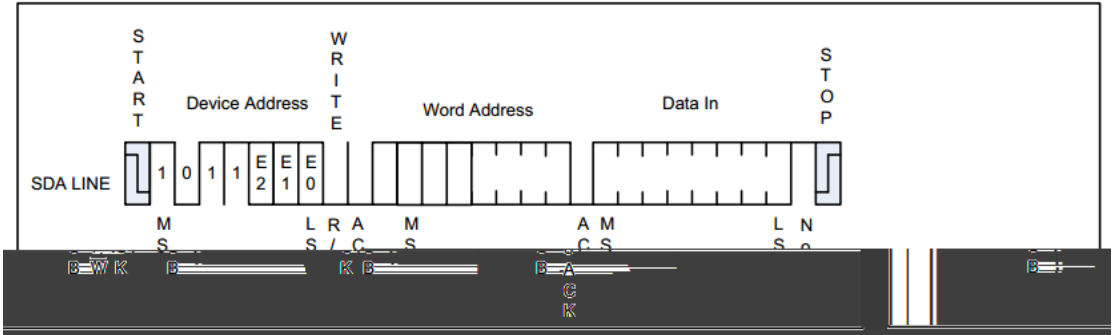
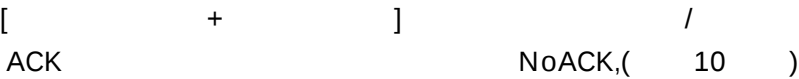
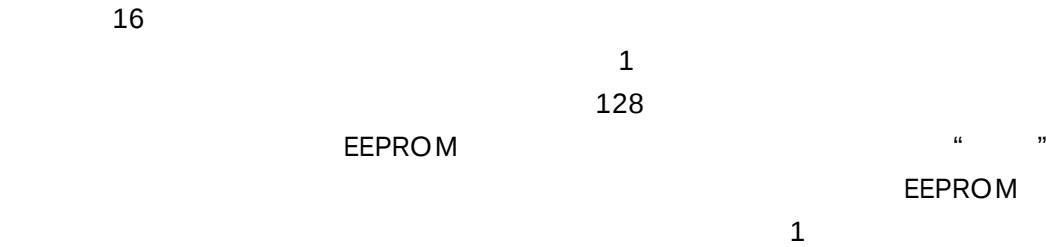


Figure 10 Lock Status Read (When Identification page locked, return NoACK after one data byte)

H



A7 A6 " 10 " 2 " 10 "
 80h
 128 16
 128 ACK
 7

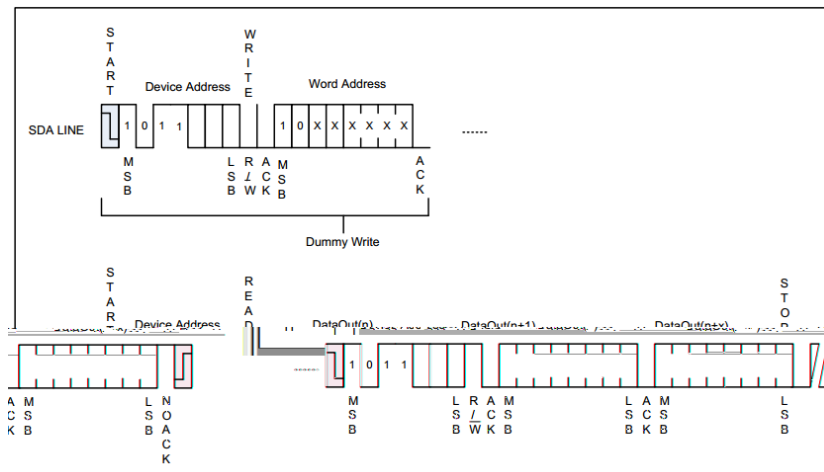
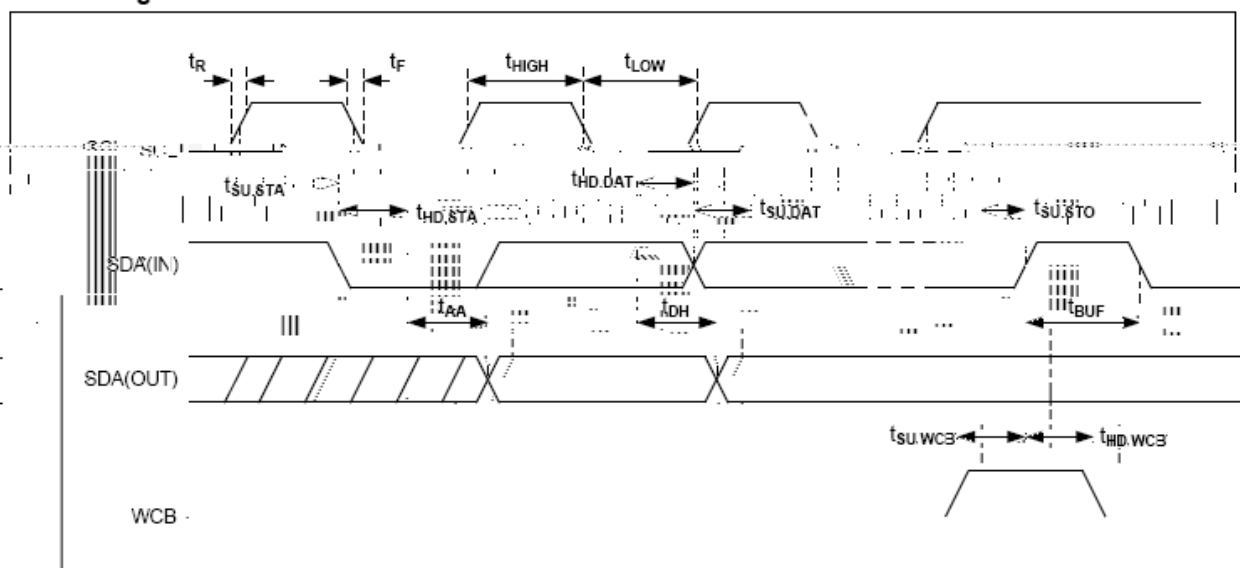
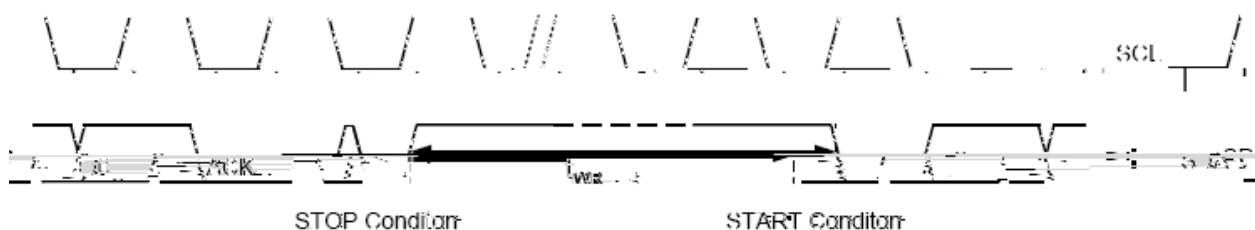


Figure 11 Sequential Read

Bus Timing



Write Cycle Timing

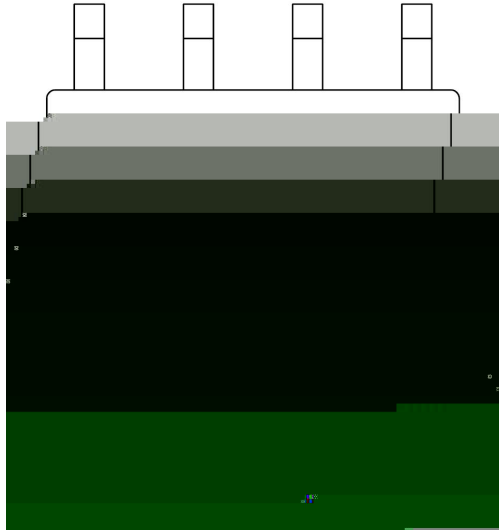


Write cycle time: t_{WC} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

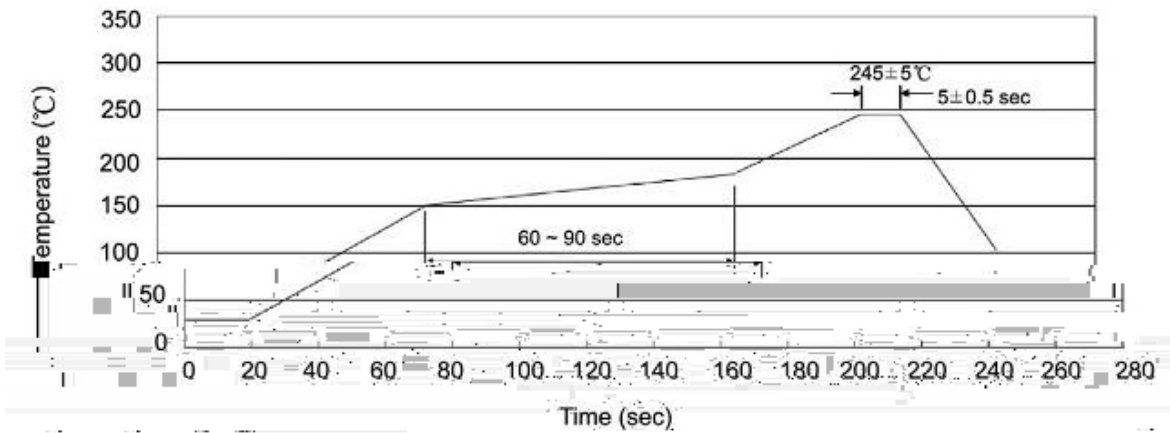
Note: The writ

1. 尺寸单位: 毫米 (除非另有说明)





24C04



± ± ± ±

± ± ± ±

封装形式	包装数量					包装尺寸		
	只 卷盘	卷盘 盒	只 盒	盒 箱	只 箱		盒	箱